In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1. (Canceled)

- 2. A computer implemented method of rasterizing a page in a page description language in a multiprocessor integrated circuit comprising the steps of:
- interpreting said page in said page description language with a first processor of said multiprocessor integrated circuit;
- spawning a subtask from said first processor to another of said processors for sorting polygon edges in increasing minimum Y coordinate.
- 1 3. The computer implemented method of claim 4, wherein:
- 2 said first processor is a reduced instruction set processor
- 3 having a floating point computation unit; and
- each of said other processors is a digital signal processor having an integer multiplier unit.
- 1 4. The computer implemented method of claim 5, further 2 comprising:
- spawning a subtask from said first processor to another of said processors for detecting a Y coordinate of edge intersection via successive midpoint approximation.
- 1 5. The computer implemented method of claim 5, further 2 comprising:
- 3 calculating a Y coordinate of edge intersection employing said 4 floating point calculation unit of said first processor.

Claims 6 to 10. (Canceled)